

**17./18. November 2016**  
**Leibniz University Hannover**  
**Institute of Microelectronic Systems**



# edaBarCamp

## 1<sup>st</sup> Contact

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Agenda / Session Wall:

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Day 1 (17.11.2016)

Time		Room 1	Room 2	Room 3	Kitchen
start	end				
10:30	10:45	Welcome & Intro			
10:45	12:00	Session Pitches			
12:00	13:00	Lunch			
13:00	14:00	Session Slot	Session Slot	Session Slot	Meeting Slot
14:00	15:00	Session Slot	Session Slot	Session Slot	Meeting Slot
15:00	15:30	Coffee & Meeting Break			
15:30	16:30	Session Slot	Session Slot	Session Slot	Meeting Slot
16:30	17:30	Session Slot	Session Slot	Session Slot	Meeting Slot
17:30	18:00	Wrap-Up & Feedback			
18:00	19:30	Spare Time			
19:30	...	Dinner & Social Nightlife			

Day 2 (18.11.2016)

Time		Room 1	Room 2	Room 3	Kitchen
start	end				
09:00	09:30	Coffee & Meeting Break			
09:30	10:30	Session Pitches			
10:30	11:30	Session Slot	Session Slot	Session Slot	Meeting Slot
11:30	12:30	Session Slot	Session Slot	Session Slot	Meeting Slot
12:30	13:30	Lunch			
13:30	14:30	Session Slot	Session Slot	Session Slot	Meeting Slot
14:30	15:30	Session Slot	Session Slot	Session Slot	Meeting Slot
15:30	16:00	Wrap-Up & Feedback			
16:00	...	End			

Summary on the 'Rules of BarCamp':

- 
- Barcamp 101 (Dr. M. Jastram):  
<http://se-trends.de/barcamp/>
  - Die goldenen Barcamp-Regeln (Hannes S.):  
<http://humanfactors-berlin.de/die-goldenen-barcamp-regeln/>

Suggestions for the Evening-Event:

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We'll go there => <http://www.gaststaette-kaiser.de>  
 Table is reserved at 7:30pm  
[www.restaurant-zwischenzeit.de](http://www.restaurant-zwischenzeit.de)  
[www.brauhaus.net](http://www.brauhaus.net)

Hints for the documentation:

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## Sessions & Documentation

- ▶ Sessions are scheduled for 45min and organized by the topic owner
- ▶ Session Breaks are 15min

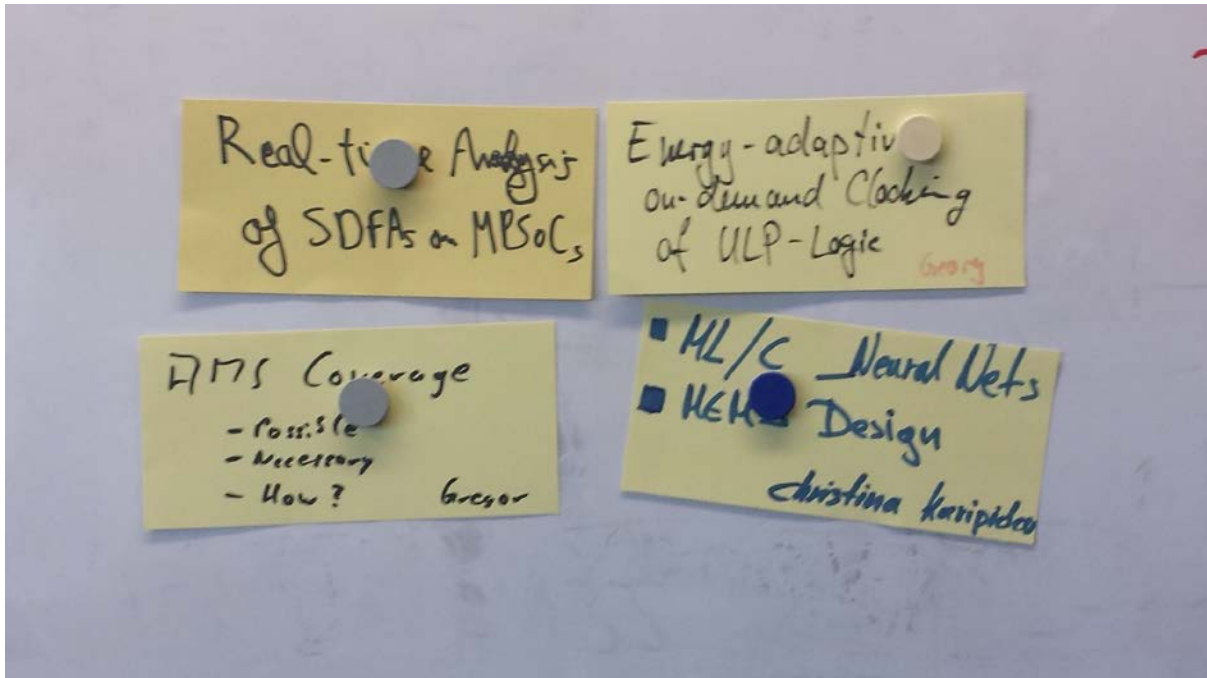
- ▶ Sessions shall be documented using

- ▶ Using Google-Docs at: <https://goo.gl/w3zvcB>
- ▶ including:

- ▶ Names and Contact data of the Session Owner
- ▶ Names of the Participants
- ▶ Selected Slides from presentations (if any)
- ▶ Photos of your Flip-Chart-, Whiteboard-Pictures (if any)
- ▶ Conclusion of your work
- ▶ Outlook to open / follow-up issues (if any)

### Session Wall for Day 1:





Session 1 (@ Library): Behavior of (EDA/Science)-PhDs concerning Facebook, Public Media, etc.

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Questions:

- is it useful to use public media / social networks to generate interest in the work on EDA science (at edacentrum)

Buzzwords:

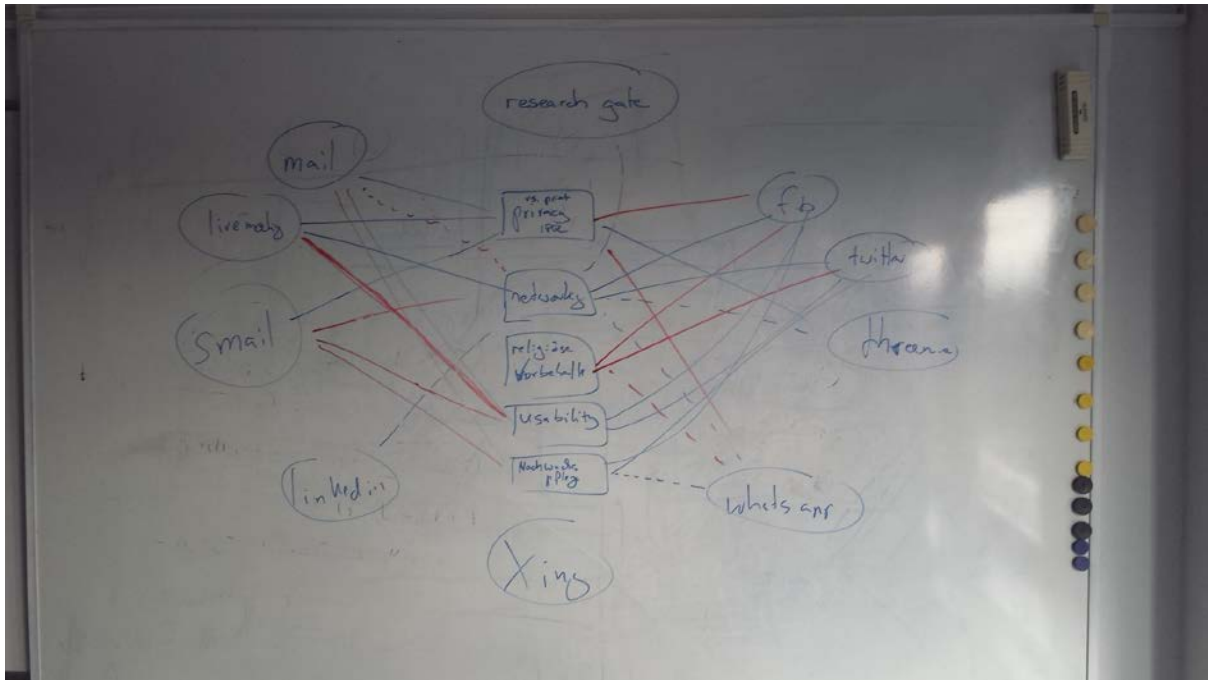
- edacentrum eda(Conference)Calendar
- Facebook (personal vs. work/science)
- platform-based (portale) vs. ...?!

Summary of possible networks:

- research gate
- facebook/Twitter
- WhatsApp
- linkedIn
- Xing

Summary of messengers:

- snailmail
- thunderbird
- threema



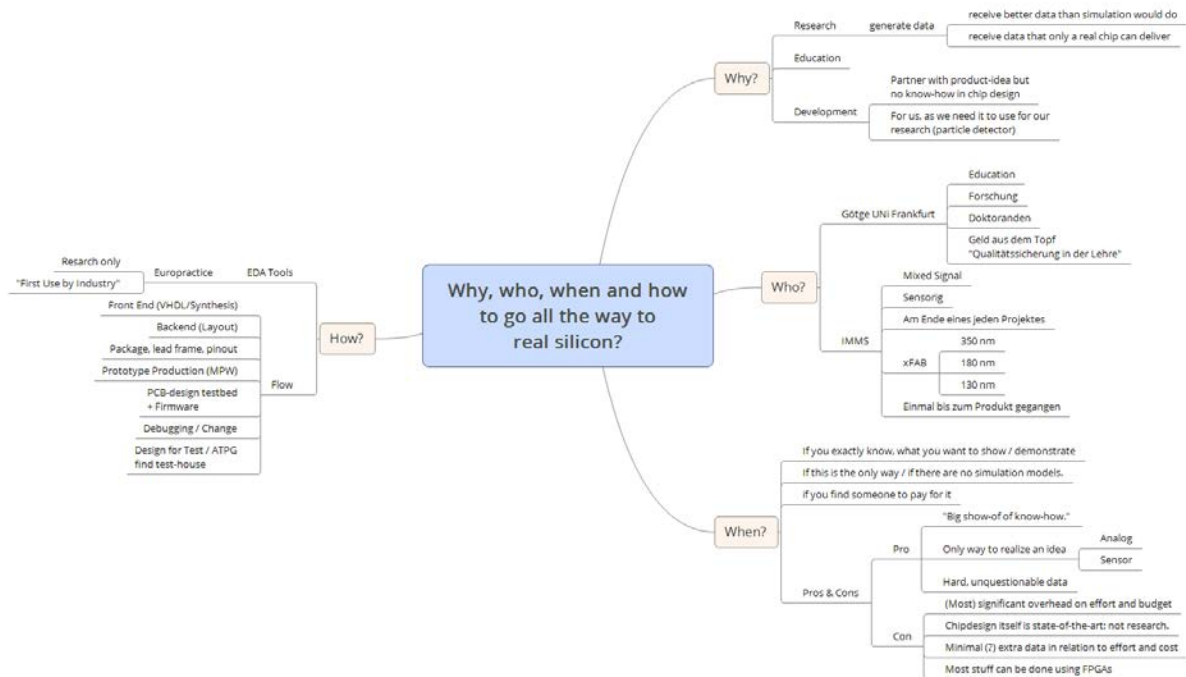
#### Use-Cases:

- Communicate Project-Calls, Call for Paper, etc.
- Public Relations (equals / is different to generating interest, awakening excitement etc.) find young applicants for eda/science
- Interesting news for newbies (e.g. Night of Science, cool technical stuff)

Marketing is everything!

The use of Facebook/Twitter in parallel to standard email will be a good idea, but the effort to do it in the right way will be high. Follow Up agreed

## Session 1 @ (conference Room): Why go all the way to silicon?



## Session 2 (@ Library): Formal AMS Verification

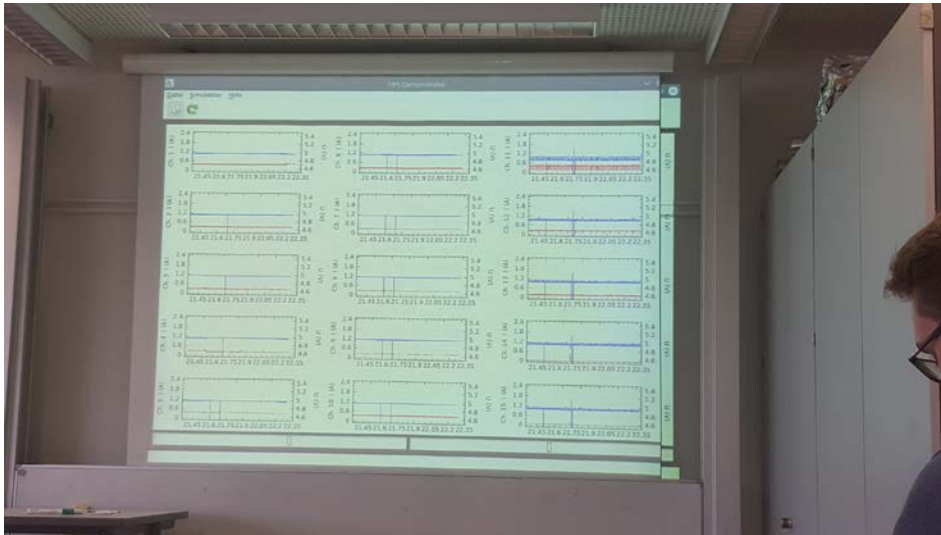
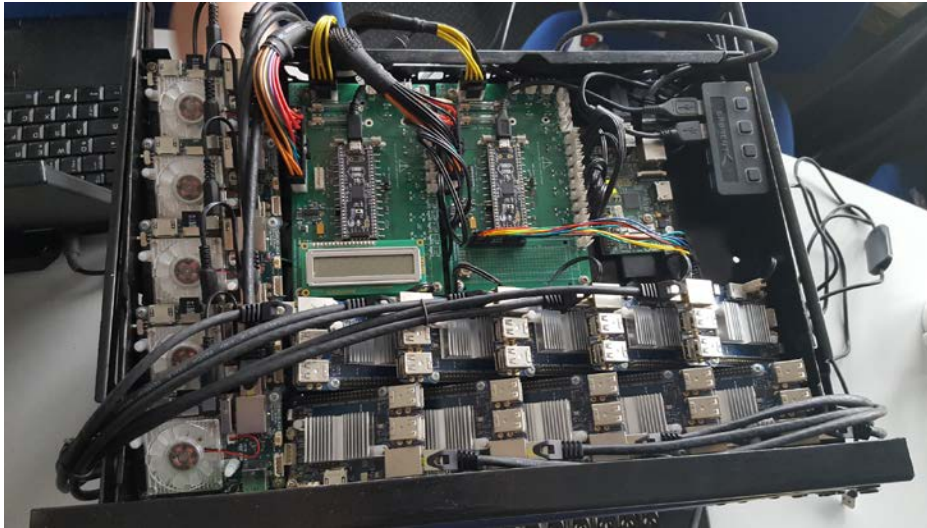
### Keywords:

- What is reachability analysis of analog circuits?
  - state space exploration
- Discretization of nonlinear analog circuits
  - MNA
  - using PRAISE approach
  - replace all non-linear devices
- What are linear hybrid systems (LHA) and hybrid systems (HA)
  - LHA: constant dynamic
  - HA: linear dynamic
- Other tools for analysis of hybrid automata: Phaver, Checkmate, Breach

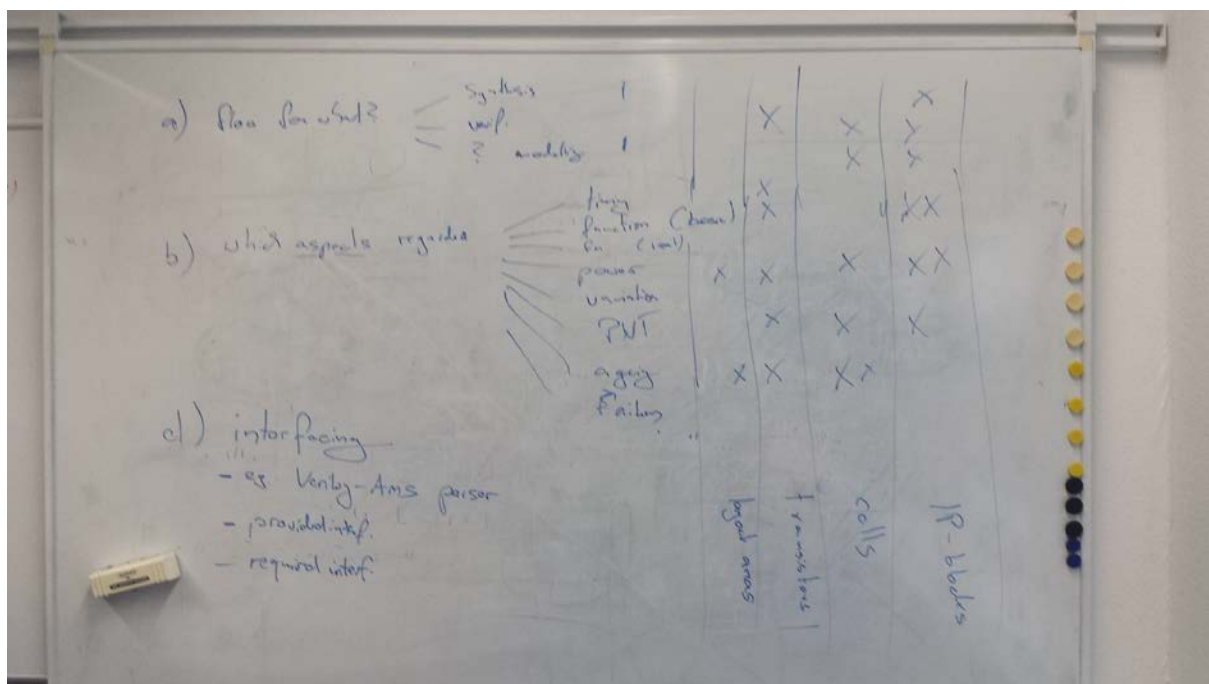
## Session 3 (@ conference room): An 80 core distributed system

Follow up agreed





## Session 3 (@ Library): Low-Level EDA



### Interfacing

- AMS Simulators are just given as a black-box -- but many ideas rely on model modification or extension
- It would be wonderful to navigate even AMS designs like in RTL-Compiler to augment/refine/... use it for new (or old) ideas, e.g.:
  - Check impedance match by extracting each block and put it into checking context
  - Refine models for verification
  - Extract parameter spaces
- We would need interface to simulation flows:
  - pre/post-simulation hooks to navigate designs, apply scripts,...
- Open source developments are difficult (up to impossible) in many projects

We are looking for straightforward possibilities to access EDA tools in detail (to access e.g. intermediate states, -data,...)

### Question for EDA-Industry

- How do you want us to participate? With abstract algorithms? or their real application? E.g.
  - by being part of EDA industry

Cadence Academic Network: Lead-University Summit @ CDNLive

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### PhD-Summit?

- like University evening @ infineon
- Socialize with managers, employes co-workes,... find collaborators for publications



### Session 3 (@ Conf. Room): Open Source Software in EDA

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- seems to be fundamentally unsolvable:
  - OSS adoption needs community
  - community needs
    - users willing to participate in development model, e.g. bug reports
    - either companies fund support due to (assumed) financial net gain
    - or individuals support software out of personal interest
  - most users are engineers, not programmers
  - result: too few companies, too few users
- another option would be research budgets reserved for follow-up support
  - but how to keep know-how present in university/r&d institute, after original researcher has graduated?

seems to be incompatible with research system as well

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### Session 4 (@ Conference Room): You use Virtual Platforms

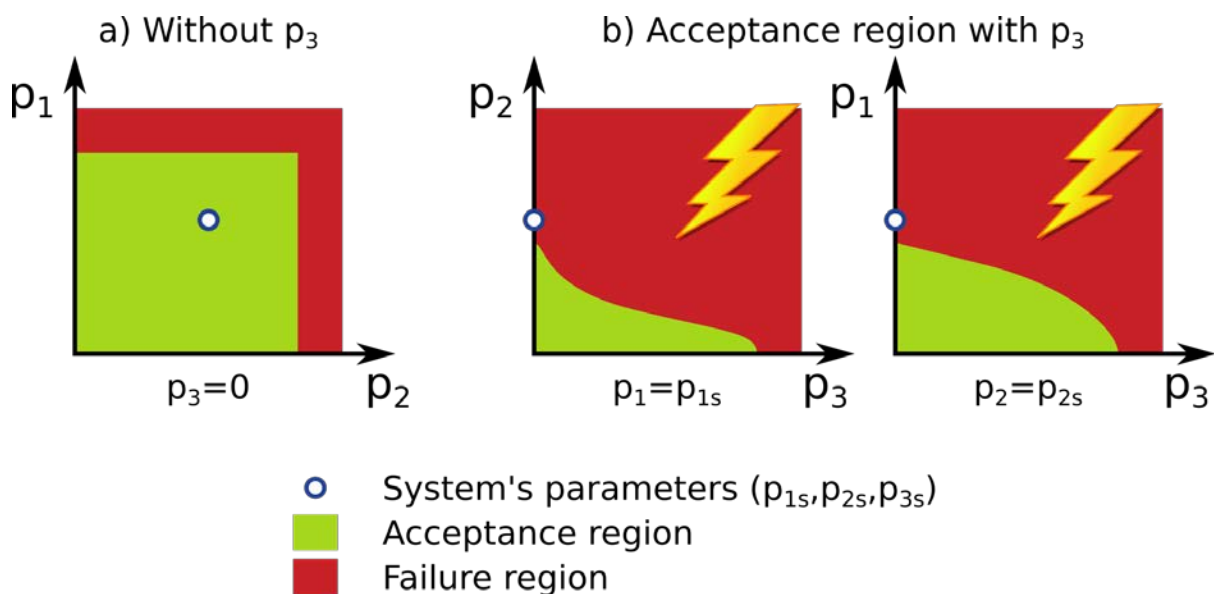
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- Christina will have a look for information what Cadence tools are available regarding virtual platforms and which features are provided
- Main question that came up: Why use virtual platforms if the real system is already available:
  - Analyzing single parts of the system/MPSoC
  - Provide informations for system designers which MPSoC/cores are right
  - Software engineer: How much power does my algorithm need, how much thermal energy does it generate
  - Analyze extra-functional properties in mixed-criticality systems in a non-invasive way, have a look insight the system
  - Goal: faster simulation with virtual platform as real embedded system
  - Co-simulation with environmental models, like at the multi-rotor demonstrator (Imperas OVP <-> iXtronics CAMEL-View Co-Simulation)

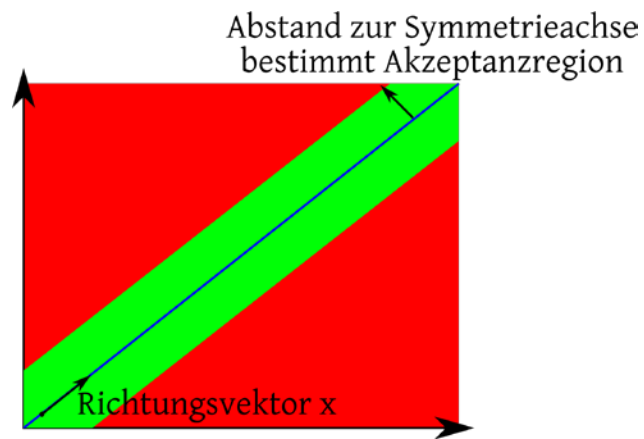
## Session 4 (@ Library): System-Level Sensitivity Analysis

- Introduction by Martin
  - Many designs are influenced by parasitic effects not included on system-level models
  - Heuristic sensitivity analysis: Distort signal and observe it's influences
  - Introduce order relation by determining tripping points
- Goal
  - Find points, where (Crosstalk, PSRR,... ) might be harmful
- Interesting Effects
  - Temperature dependent effects
  - Local or global variation
  - Aging  $\Rightarrow$  e.g. Raise threshold voltage of transistors
  - Offsets
  - Nmos/Pmos Corner-values
  - SEU, ionizing radiation
- Detection of Dependencies:
  - Linear neural net  $\rightarrow$  map back to matrix equation (should approximate separating surface)

To detect constraints, the obtained regions have to be examined/approximated. In the following picture, this can be done using a linear classifier.



Symmetry-constraints can not be found like this, additional "tricks" have to be applied.  
 $\Rightarrow$  Additional non-linear input quantities for the classifier



Since the distance to the symmetry axis is the criterion to be examined, this should be an input quantity. It can be expressed for some point  $b$  and span-vector  $x$ :

$$d = \|b - x^+b\|$$

The direction of  $x$  can be obtained from the shown region.

2nd Day (Session pitch)

	Conference Room	Library	Kitchen
10:30 - 11:30	<p>Chances &amp; Possibilities of formal Verification in RDS / System Design</p>	<p>Applications for highly parallel embedded systems</p>	<p>Group Photo (for IET as a group)</p>
11:30 - 12:30	<p>RTM Coverage</p> <ul style="list-style-type: none"> <li>- results</li> <li>- accuracy</li> <li>- how?</li> </ul>	<p>H200 C/C++ Brainstorming</p>	<p>Virtual Platforms for analysis Extra. Functional properties + Real Time constraints</p>
13:30 - 14:30	<p>PhD in EDA</p> <p>Hou 2 @ AN ACTIVE SM-based EDA Community → PARTICIPATE!</p>	<p>Methodology for solving shell in ARM Design</p>	<p>Energy-adaptive on-demand blocks of ULP-Logic</p>
14:30 - 15:30	<p>Co-design of VHDL</p>	<p>Real-time Analysis of SDF in ASICs</p>	<p>Let's talk about Java's Mini PC</p>
Feedback		<ul style="list-style-type: none"> <li>■ H2/C Shared Uets</li> <li>■ MEMS Design</li> </ul> <p>christina.karpis</p>	

## Session 1 (@Library): Applications for highly distributed embedded platforms

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NoC is related, and has the same problem: Solutions in search of a problem

- Car (certification is problematic)
- Sensor networks (which ones?)

Error resilience: performance required by algorithms cannot be met with technology that is aging resilient (3y until failure will not be used in car)

- multiple mappings to allow n communication/ECU failures without degradation
- ... with degradation, turn off services selected by priority

Final verdict: keep eyes & ears open for a matching call/industry partner

## Session 1 (@ Conference Room): Need, Possibility and Chances for Formal Verification in AMS/System-Design

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### Need for AMS-Verification:

- yes (theoretically)
- no (practically, because of its limits... maybe at the system level of interactions between AMS components)

### Problems:

- understanding of algorithms and languages
- AMS Designers are (still) thinking in Schematics and Layouts (Transistors) → Programming/Programs/Computer Scientists are different way of thinking
- Complexity: at Layout-Extracted-Level (complex MNAs) vs. Schematic-Level (less complex MNA) → checking equivalence maybe possible using Symbolic Analysis for Model Order Reduction and checking the error, introduced by the reduction
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### Question:

- adaption / interfacing between schematic based thinking and formal verification (models / specifications / properties)

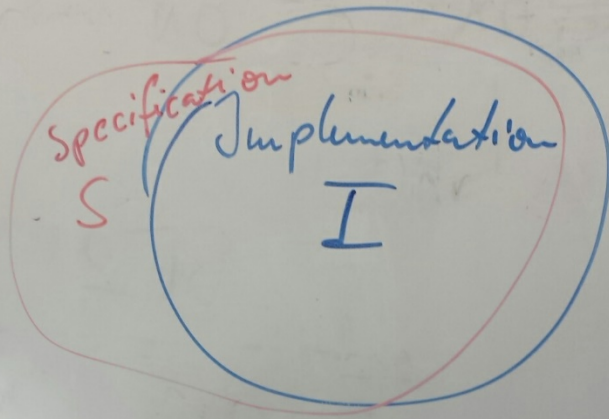
### Methods:

- equivalence checking
  - LVS is already there ;) ⇒ does not include parasitics (can only be extracted and simulated)
- Idea:  
Could symbolic simplification techniques (for MNA as eg Analog Insydes is using) be used for verification
  - Use this to evaluate the error between schematic and layout MNA?

Cadence Tools: Assembler, Verifier, Explorer

[https://www.cadence.com/content/cadence-www/global/en\\_US/home/solutions/mixed-signal-solutions/mixed-signal-verification.html](https://www.cadence.com/content/cadence-www/global/en_US/home/solutions/mixed-signal-solutions/mixed-signal-verification.html)

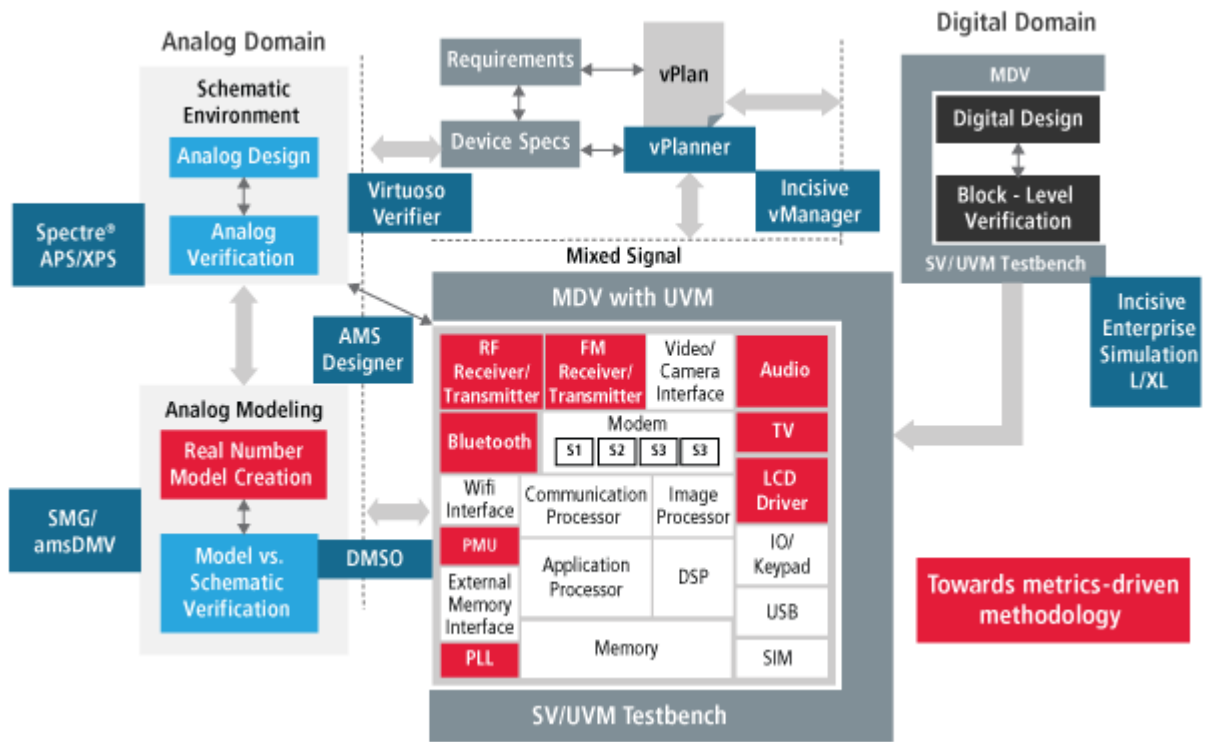


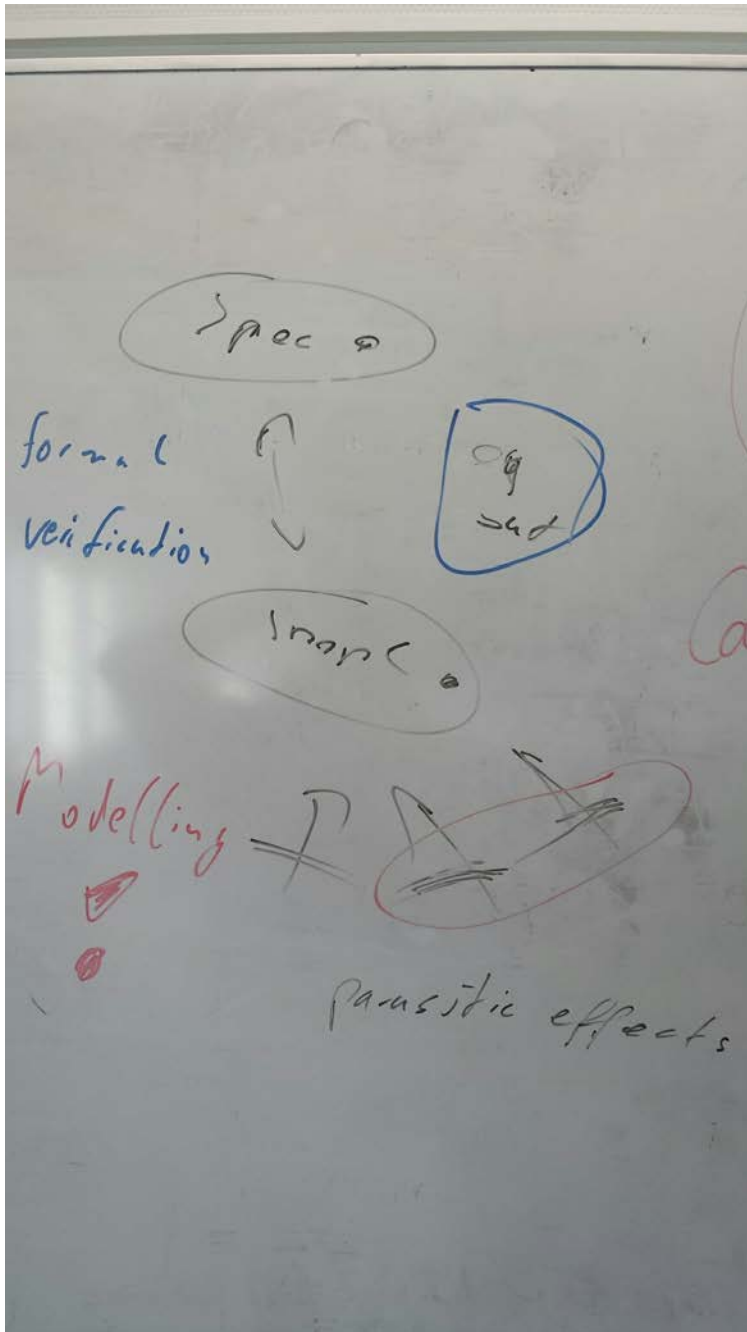


Can we formally prove  
 $S = I$

$S$

$\neq S$





Session 3 (@ Conference Room): AMS-Coverage

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WER & WOHIN: edaCentrum, Forschungs-/Industriepartner, Individuen (Prof., PhDs, Studs)

WAS:

Bingo-Phrases

- I agree a little bit, but I disagree a little bit more
- Wenn ein Modell einen falschen Ausgang hat ...

## Session 2 (@Library): Ideas for an ICT 2017-05 proposal

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Main problem: 2 complementary applications called for

Application Ideas:

- Mission Profiles in automotive are sufficiently complex and desired by manufacturers
  - what about certifiability?
- Smart Home not too convincing
- Drone Fleets? (not existing yet)
- Autonomous Car fleets?

Link to call:

<https://ec.europa.eu/research/participants/portal/desktop/en/opportunities/h2020/topics/ict-05-2017.html>

## Session 3 (@Library): CFP8 & OpenSource

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Development of an OpenSource Infrastructure for Mixed-Signal Circuits

Who could be included?

- IMMS
- Offis
- LUH
- UFFM?

Goal:

- Create Infrastructure like libClang for Mixed-Signal Circuits to navigate, extract, modify a given model and simulate it
- Processing model as transformation on XML/XSLT
  - Parsing frontend to emit XML that can be processed by tools
  - Has to be transferred back to code
  - Example: Refactoring, Structure extraction, Syntax, Property extraction

## Session 3 (@ Conference Room): Facebook / Public Relations / Communication for EDA Community

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### Questions:

Who will communicate?

Who will read?

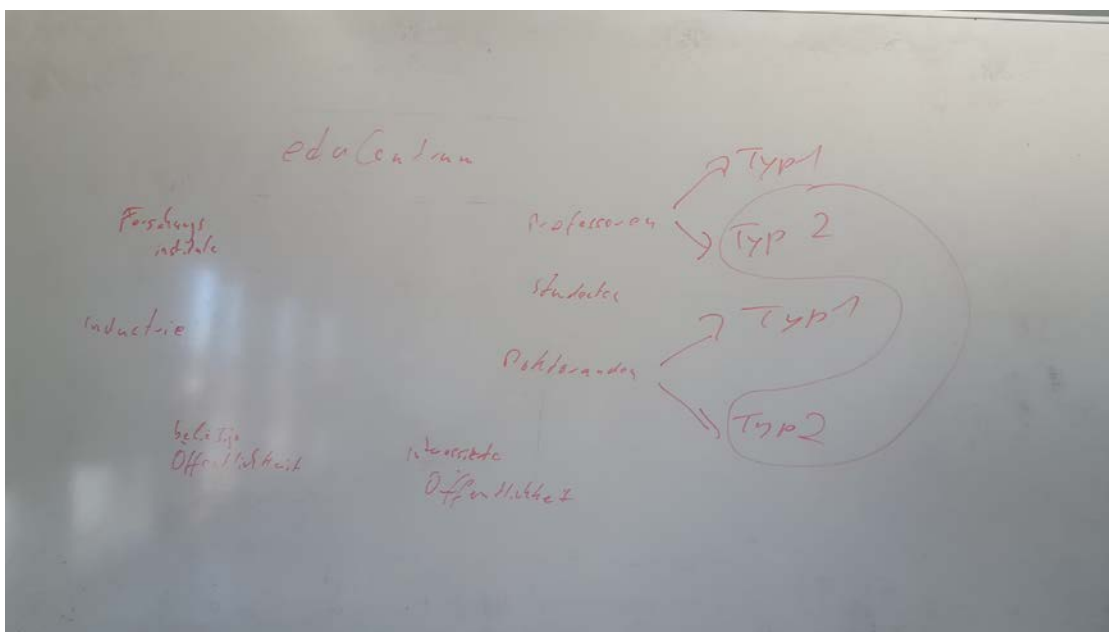
What should be communicated?

### Suggestion:

We should try Facebook in combination with Twitter

We have to build an emotional relationship between edacentrum and the followers (can be reached better with emotional posts than with product releases....)

1. Step: edacentrum will post information like edaCalendar (www.edacentrum.de/edakalender), Call for Papers, BMBF calls, News,... - but also emotional news (e.g. sunset over the edacentrum building, new staff member, fotos from the Christmas party, .....)
2. edacentrum has to promote the use of Facebook to get more followers.
3. Step: when a critical size of followers has been reached it can be interesting for persons to post something on the edacentrum Page.



We need a communication matrix : Who will communicate with whom?

It is needed to fill in the matrix within the next steps...

Good Facebook website: FESTO

Open questions:

Duzen oder Siezen (you can say you to me...)? Approval necessary for every posting?

Session 4 (@ Conference Room): Cadence EDA-tools and Summit possibly at CDN Live 2016

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Maybe have some kind of BarCamp-Session @CDNLive?

Cite:

Hi,

I have prepared a short survey regarding the Cadence Academic Network Summit. Please visit <https://www.surveymonkey.de/r/GWPHTNL> to submit your answers.

If you have any questions or comments please contact me at [ckaripid@cadence.com](mailto:ckaripid@cadence.com)



## Summary of the participants' feedback

9 of 14 Participants answered the following Questions:

Q1: Did you liked the event? (Why?)

Q2: Would you participate again? (Why?)

Q3: My highlight / lowlight of the event was ...

Q4: My suggestions to further improve the event are ...

Question	Yes	No	--	Sum
Q1	9	0	0	9
	<ul style="list-style-type: none"> <li>- Interesting topics &amp; discussions (5)</li> <li>- Nice people, nice atmosphere (3)</li> <li>- Constructive and interactive concept (2)</li> <li>- Diversity of topics and viewpoints (2)</li> <li>- Educative</li> </ul>			

Question	Yes	No	--	Sum
Q2	7	0	2	9
	- Same reasons as for Q1			

Question	Highlights
Q3	<ul style="list-style-type: none"> <li>- topics &amp; discussions (3)</li> <li>- Session Pitch &amp; Scheduling Session</li> <li>- Feedback on Cadence EDA tools</li> <li>- Get-together / Networking / Nightlife (3)</li> <li>- H2020 proposal</li> <li>- Learned the BarCamp-Mode</li> </ul>
Question	Lowlights
Q3	<ul style="list-style-type: none"> <li>- Could not attend every interesting session / missed the demonstrators (2)</li> <li>- Affiliation diversity</li> </ul>

Question	Suggestions
Q4	<ul style="list-style-type: none"> <li>- Better PR to get more people and more topics (4) <ul style="list-style-type: none"> <li>→ send printed posters / flyers to universities / institutes</li> <li>→ propose ,local edaBarCamps' to spread the label</li> <li>→ ,Steering Commitee', known Profs, success stories</li> </ul> </li> <li>- Better Date: no trade fair → cheaper hotels (3)</li> <li>- Keep in touch (3) <ul style="list-style-type: none"> <li>→ facebook groups, mailing lists, etc.</li> </ul> </li> <li>- Emphasize the availability of ,Free Meeting Slots' without a topic</li> <li>- Add 1 additional slot at day 1</li> <li>- Get more people and partition into dedicated topic areas</li> <li>- Don't grow too large to manage the session pitch</li> </ul>